SIMS Analysis of Oxygen Impurity levels when using Point-Of-Use Hydrogen Purification in a Silicon Germanium epitaxial deposition process for a Strained Silicon application

Raj Chakraborty, Pall Corporation Scientific and Laboratory Services Department, Port Washington, NY

Abstract

A Pall Maxi-Gaskleen™ purifier of the Pall AresKleen™ family of gas purification products was evaluated for its efficacy in reducing oxygen impurities in a silicon germanium (SiGe) deposition process for a strained silicon application at a major IDM in the US. Impact on process parameters such as hydrogen pre-bake temperature and interfacial/within-film oxygen concentration were studied as a function of hydrogen purification. All film impurity analysis was done using SIMS techniques. The study showed that the Maxi-Gaskleen purifier should be effective in preventing impurity spikes that are responsible for elevated levels of oxygen in the SiGe film and the SiGe/Si interface from entering the reactor. The hydrogen gas is used in the high temperature pre-bake step of the SiGe epitaxial deposition process.

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1. Introduction

With low power dissipation, high integration levels, good noise immunity, and high cost-effectiveness, silicon CMOS technology occupies a dominant position in microelectronics. However, the low mobility of electrons and holes in silicon limits its application to relatively low frequencies, leaving III-V materials such as gallium arsenide and silicon germanium to fulfill roles in high frequency applications. Lots of effort has been made to improve carrier mobility and thus, the speed of MOS transistors. Strained Silicon technology has emerged as the leading candidate to address these problems. As opposed to conventional line-width reduction solutions, strained silicon technology offers a radical enhancement to the current drive capability of devices. The technology is successfully moving into high-volume manufacturing and holds even greater promise for future acceptance due to its incorporation into mainstream processes at several major IDM's.

The Pall Maxi-Gaskleen purifier used in this study contains a proprietary purification material that removes impurities by four mechanisms: direct chemisorption, dissociation of the impurity followed by dissolution or reaction with the purification material, chemisorption of reaction products, and chemisorption and/or physisorption on the substrate. Prior analytical test data[12] has revealed a strong affinity of the purification medium towards impurities like oxygen, moisture, carbon dioxide, and carbon monoxide in various gases including hydrogen. The purifier has exhibited effective removal of these impurities to sub ppb levels from ppm levels, with a good removal capacity for such impurities. Furthermore, the purifier is integrated with the Pall Ultramet-L® filter that is effective at removing particles down to 3nm with 9-log efficiency.

1.1 What is Strained Silicon and how is it processed?

Because silicon has a smaller lattice constant (atom spacing) than SiGe, when silicon is grown on SiGe, the silicon lattice is stretched,

forming a strained layer, as shown in Figure 1. This strained silicon layer serves as the channel for transistors fabricated thereafter.

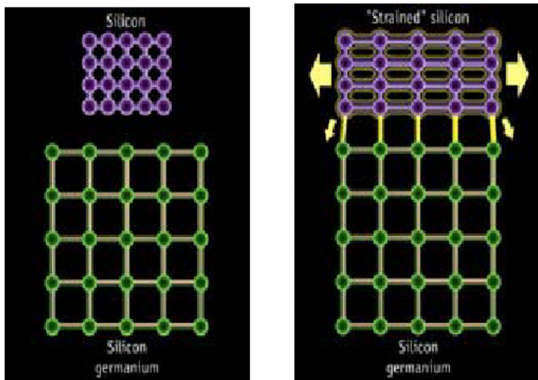
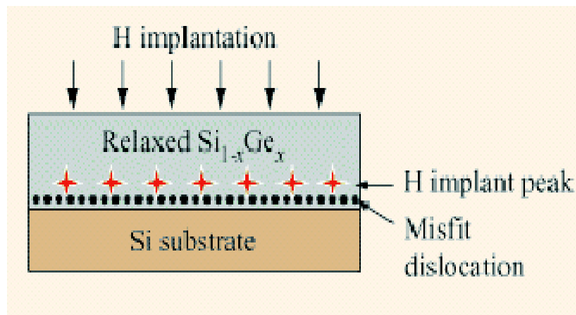


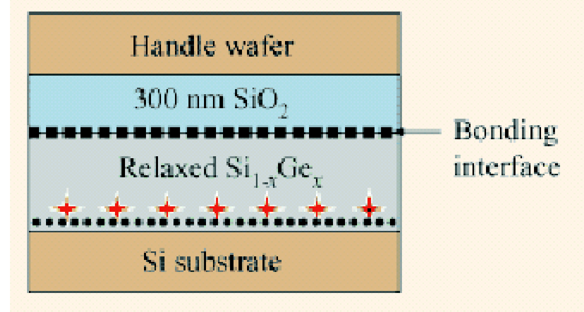
Figure 1: Strained (stretched) Silicon on Silicon Germanium[1]

A simplified basic version of the process of fabricating a strained silicon transistor is as follows:

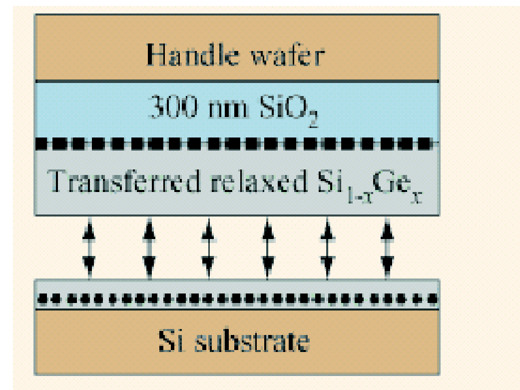
1. Epitaxial deposition of a SiGe film (called the relaxed SiGe layer) on a silicon substrate. This wafer is referred to as the substrate wafer.[1-2]
2. Hydrogen Implantation to form a cleave layer followed by a thermal activation of the implanted ions.[1-2]



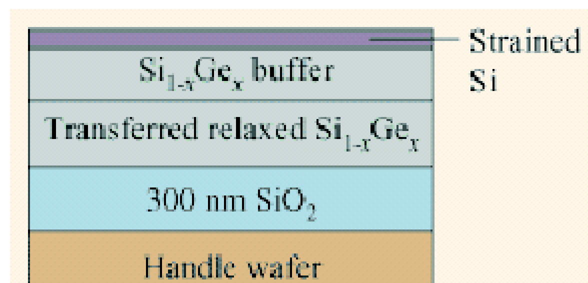
3. A separate oxidized silicon wafer (Handle wafer) is bonded to the surface of the SiGe on the substrate wafer.[1-2]



4. The bonded wafers are cleaved at the Hydrogen Implant layer.[1-2]



5. SiGe surface is CMP polished as micro-roughness in this layer transmits into the strained silicon layer grown on top of this causing decrease in carrier mobility.[1-2]
6. SiGe buffer layer is grown and this is a graded layer, i.e., the Ge content is varied across the depth of the film as this has been shown to enhance carrier mobility.[3]
7. Strained silicon is epitaxially grown on this SiGe buffer layer and serves as the active base for devices fabricated on it.[1-2]



While there are other processes that are used to fabricate strained silicon structures, the aforementioned Silicon Germanium On Insulator (SGOI) is the most common.

The purpose of the oxide layer is to reduce junction capacitance and to render the device latch-up resistant. These parameters affect the frequency operation and reliability of the device.

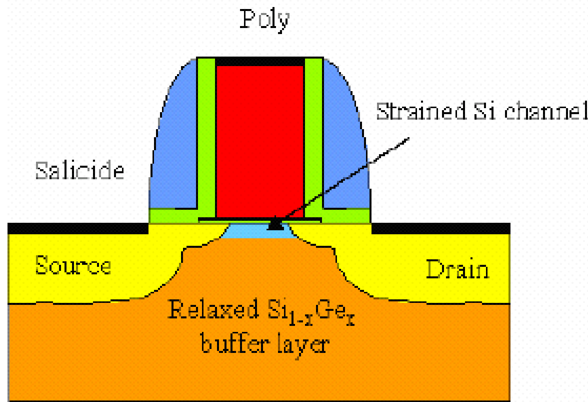


Figure 2: Cross section of a finished NMOS transistor on a strained Silicon substrate[2]

2. Experiment and Results

A Pall Maxi-Gaskleen™ purifier (Part No. GLP8SIPVMM4) was used in purifying the hydrogen gas used in the epitaxial deposition of the SiGe film in a state-of-the-art epitaxial reactor. The hydrogen was used for the high temperature pre-bake prior to deposition.

SIMS analytical techniques were used to monitor the oxygen levels at the Si/SiGe interface and within the SiGe film. These tests were all done at the customer's facility.

Figure 3 shows the SIMS analysis of a SiGe film epitaxially grown with point-of-use (POU) purified hydrogen as a pre-bake gas. The Pall Maxi-Gaskleen purifier was installed on the hydrogen line and after appropriate conditioning, the following SIMS analysis was conducted on a product wafer. The other elemental curves were not calibrated during the analysis, hence should be ignored.

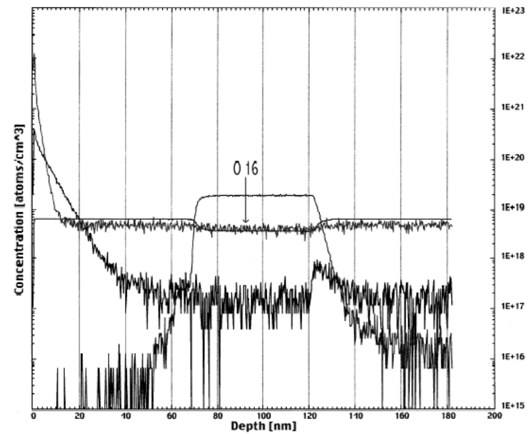


Figure 3: SiGe SIMS data after installation of a POU purifier on the hydrogen gas line

The customer also reported that they had seen an impurity spike - oxygen concentration levels of around 1E20 atoms/cm^3 in the SiGe film (60 nm SiGe film: 70 nm – 130 nm) and around 2E19 atoms/cm^3 at the SiGe/Si interface (SiGe/Si interface: 130 nm – 140 nm) - at one prior occasion, when there was no POU purifier in place on the hydrogen line. As a result of this impurity spike, the customer had to temporarily increase the hydrogen bake temperature for the duration of the spike in order to lower the oxygen levels. Once the process returned to normal conditions, the temperature was decreased. It should be noted that this epitaxial reactor was being used for research and development work and hence variations in the process could somewhat be compensated for. However, if this were a production tool, such process variation caused by varying impurity levels in the hydrogen line would result in yield losses.

Upon analysis of the SIMS data and of the reported impurity spike information, one could deduce that having a POU purifier on the hydrogen line would ensure that the oxygen levels in the SiGe film and the SiGe/Si interface stay at 5E18 atoms/cm^3

levels (from Figure 3). Without effective POU purification, impurity spikes, which are known to occur from time to time in gas lines, could make it into the reactor. Data with oxygen concentrations in a SiGe film grown with POU purified hydrogen gas during such an impurity spike could not be achieved due to lack of such a spike in the hydrogen line during the POU purifier installation and testing.

3. Discussion

Before the SiGe film is deposited on the silicon wafer, chemical and native oxide has to be removed from the silicon surface. The source of the chemical oxide is usually from a wet clean performed prior to the epitaxial deposition to ensure that the surface is free of any contaminants prior to epitaxial deposition. This oxide can be removed by several methods. The most preferred way of doing this is by an in-situ high temperature hydrogen bake prior to the SiGe deposition. This ensures that no native oxide grows between the oxide removal and epitaxial deposition steps. This works by converting the surface oxide to volatile sub-oxides (e.g. SiO), which sublime from the wafer surface.[4]

The hydrogen bake is typically performed between 850°C and 900°C for 30 seconds to 60 seconds and is usually performed at the same temperature as the epitaxial deposition to improve throughput of single wafer reactors. For this bake to be effective, the partial pressure of O_2 and H_20 within the reactor must be low enough so that the existing oxide is no longer stable and new oxide is not formed. The partial pressure of the O_2 and H_20 within the reactor is proportional to the levels of O_2 and H_2O impurity in the hydrogen gas and hence, ultrapure hydrogen has to be used for this process.

Despite the high purity of the hydrogen gas (obtained from boiling a liquid source and subsequently purified at the gas cabinet) at the customer's facility, POU purification was necessary to achieve sub-ppb levels of O_2 and H_2O in the hydrogen gas as it entered the reactor. The customer had noticed a spike in the oxygen levels in the SiGe film and at the SiGe/Si boundary prior to installing POU purification. This was monitored by SIMS analysis and indicated that the hydrogen bake was not completely successful in removing the chemical and/or native oxide during these spikes. This meant the partial pressures of the O_2 and H_20 impurities in the reactor (from the hydrogen) had increased, thus decreasing the effectiveness of the bake. This resulted in a thin oxide remaining at the boundary and furthermore, resulted in higher than normal oxygen levels in the SiGe film. Such oxygen levels in the film are known to have undesirable effects on device performance by contributing to mobile charges that can migrate to active device regions during the epitaxial deposition process.[2] Furthermore, they are also known to cause shifts in breakdown voltage and leakage current in the film.[3,6] In heterostructure devices using SiGe, such oxygen levels would prove to be disastrous by contributing to undesirable interface trap charges.[7-9,11] Interface trap charges are not as detrimental in strained silicon processes. To address such occasional spikes, the customer had to raise the hydrogen bake temperature to ensure complete removal of the interface oxide and reduce the oxygen levels in the SiGe film. As a consequence, the deposition temperature would have to be increased to ensure high throughput.

A higher temperature process is not desirable in this case, as in most other semiconductor processes, from various thermal budget perspectives. The most significant factors are the need for a lower growth rate for better process control and uniformity of thin films and the need for reduced dopant segregation to ensure steep abrupt dopant profiles.

After installation of the POU purifier on the hydrogen line, such an impurity spike associated with the O_2 and H_2O impurities

was not seen. This translates into a stable and steady bake temperature and constant oxygen levels in the SiGe film, which in turn greatly helps reduce process variation. This also eliminates the need to raise the bake temperature and leads to increased predictability of device performance, which depends on the quality of the underlying SiGe film. Also, oxygen and other impurities are known to alter the lattice structure of the deposited film if they are present in sufficient levels[4-5]. The relaxed nature of the non-buffer SiGe film is important from a bonding perspective as outlined in the process flow above. If the film is not sufficiently relaxed, stress micro-cracking and poor adhesion can result in improper bonding of the substrate and handle wafer. Impurities in the deposited film are also known to reduce the relaxed level of the film and to induce undesirable stress within the film.[9-10]

Having a POU purifier in place right before the hydrogen entered the reactor also offered the customer the security of not having any kind of impurities or particles (that may have degassed or shed from the gas lines, gauges, or cylinder) enter the chamber during normal operation or during system maintenance. Such impurity spikes in the gas line are not unusual during system PM's or normal system operation. It should also be noted that POU purifiers were already in place for all the other gases feeding the reactor. The hydrogen gas line was the only line devoid of any POU purifier.

Experiments done by the customer to test the oxygen levels at the Si/SiGe interface as a function of the bake temperature revealed some interesting results. A 20°C increase in the nominal bake temperature reduced the oxygen levels at the interface by 87.5%. To reduce the oxygen spikes encountered from time to time in the aforementioned SiGe deposition process, a 20°C – 25°C increase in the bake temperature would be needed. This is evident when taking into consideration the oxygen levels in Figure 3 and those reported during the impurity spike.

4. Conclusion

Based on the data obtained from this evaluation and additional impurity removal efficiency test data[12] that exists on this product, the Pall POU hydrogen purifier would help in inhibiting an impurity spike in the gas and/or in the gas line from entering the reactor. Furthermore, process and device variation and predictability are improved as a result of such impurity removal. Also noteworthy is the fact that along with molecular impurity purification, particle removal is also gained by this POU technology. Effects of particle removal on the SiGe deposition process were beyond the scope of this study. Applications other than strained silicon technology, most notably raised source/drain structures due to the low temperature SiGe deposition process, are also likely to see similar benefits from the aforementioned improvements to the SiGe epitaxial deposition process. With the trend towards low temperature SiGe deposition, such process variation and the associated impurities will be more of a concern.

5. References

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